EAST - [10815860.wsp:1]

File View Edit Tools Window Help

- Drafts
- Pending
- Active
  - L1: (4) (multi-layer near substrate multi adj layer adj substrate) and reduc$3 near layout
  - L2: (4) (multi-layer near substrate multi adj layer adj substrate) and reduc$3 near layout
  - L3: (65) (multi-layer multi adj layer) and reduc$3 near layout and substrate
- Failed
- Saved
- Favorites
- Tagged (0)
- UDC
- Queue
- Trash

Search | List | Browse | Queue | Clear

DBs | US-PGPUB; USPAT; USOCR; EPO; JPO | Plurals

Default operator: OR | Highlight all hit terms initially

(multi-layer multi adj layer) and reduc$3 near layout and substrate

BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
39	☐	☐	US 6678184 B2	20040113	13	CAM cell having compare circuit formed over two active regions	365/49	365/156; 365/189.07
40	☐	☐	US 6662344 B2	20031209	34	Semiconductor device and method for fabricating the same	716/1	257/E21.564; 257/E21.703; 257/E27.112;
41	☐	☐	US 6645790 B2	20031111	24	System and method for prototyping and fabricating complex microwave circuits	438/107	438/110; 438/17; 438/64;
42	☐	☐	US 6573964 B1	20030603	38	Multidomain vertically aligned liquid crystal display device	349/129	349/138
43	☐	☐	US 6553044 B1	20030422	20	Method and apparatus for reducing electrical and thermal crosstalk of a laser array	372/38.02	372/34; 372/50.12
44	☐	☐	US 6552360 B1	20030422	10	Method and circuit layout for reducing post chemical mechanical polishing defect count	257/48	438/139; 438/626; 438/690;
45	☐	☐	US 6414381 B1	20020702	14	Interposer for separating stacked semiconductor chips mounted on a multi-layer printed circuit board	257/676	257/686; 257/724; 257/787;
46	☐	☐	US 6392942 B2	20020521	36	Semiconductor memory device having a multi-layer interconnection structure suitable for merging with logic	365/205	257/E27.097; 365/230.03
47	☐	☐	US 6380589 B1	20020430	17	Semiconductor-on-insulator (SOI) tunneling junction transistor SRAM cell	257/347	257/354; 257/57; 257/59;
48	☐	☐	US 6209123 B1	20010327	114	Methods of placing transistors in a circuit layout and semiconductor device with automatically placed transistors	716/14	716/11; 716/12; 716/13;
49	☐	☐	US 6140705 A	20001031	6	Self-aligned contact through a conducting layer	257/774	257/758; 257/773; 257/E21.577;

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